Questions for self assessment

Module 11--Lecture 1

1. What does BIST stand for?

2. Why do we require BIST even after all circuits are tested before deployment?

3. Draw and explain the basic architecture of BIST.

4. We know that in BIST, hardware pattern generator is required. Ideally speaking, the pattern generator should be able to generate the exhaustive set (i.e., generate all patterns from 0 to 2^n, if there are n flip-flops in the register). A simple counter can do it. But in BIST, counters are not used as pattern generators, why?

5. Suggest circuits which can be used as pattern generators in BIST.

6. Outputs of the circuit under test in case of BIST need to be compressed, why?

7. Discuss some output compression techniques used in BIST.

8. What are the issues with output compression in terms of test coverage?

Module 11--Lecture 2,3

1. Why we consider testing of memory chips different compared to other digital (combinational/sequential) circuits?

2. What are the popular memory fault models? Among the memory fault models which are the ones that are different for the ones considered in other digital (combinational/sequential) circuits?

3. What are the different types of neighborhood considered for memory fault models?

4. What is March test?

5. Which memory faults cannot be detected by March test? How can those faults be detected?

6. Why is BIST of memory important?

7. What is the basic difference between pattern generators used in memory BIST compared to BIST of ordinary (combinational/sequential) circuits?